Vlsi Design

VLSI

SYLLABUS

COVERAGE

- VLSI design flow and methodologies
- FPGA architecture
- Digital Logic Creation Techniques
- Real Life Event Logic Design(Traffic Light Control,
- Three Way Switch, Car Locking)
- Digital Electronics logic design
- Verilog coding
- Synthesis and Verification
- Advanced Digital electronics circuit design using FSM
- CMOS fundamentals
- CMOS circuit design
- Layout Design
- Industry Oriented Projects
- IP design methodologies
- Next generation Transistor(TFET study)

SYLLABUS IN DETAILS

Introduction
- What is VLSI?
- Introduction to CMOS technology
- Demanding area for company
- Application of VLSI
- Indian ESDM market-Analysis of Growth &
- Opportunity Plan
- VLSI design methodologies
- VLSI Design Flow

Digital IC Design
- Overview of Digital Design with Verilog HDL(Day-2)
- Evolution of Computer Aided Digital Design
- VHDL vs Verilog
- Importance of Hardware Description Language(HDL)
- Popularity of Verilog HDL
- FPGA Architecture
- FPGA vs ASIC

Hierarchical Modeling concept
- Design of 4-bit ripple carry adderModules
- Instances
- Components of a simulation
- Example: Design Block, Stimulus Block

Gate-Level Modeling
- Gate types
- Gate Delays

Tasks and Functions
- Difference Between task and function
- Tasks
- Automatic(Re-entrant) task
- Functions
- Automatic(Recursive) function

Useful Modeling Techniques
- Procedural Continuous Assignments
- Use of force and release
- Overriding Parameters
- Conditional Compilation and execution
- Time Scale
- Useful system tasks

Dataflow Modeling
- Continuous Assignments
- Delays
- Expressions, operators and operands
- Operator type
- Design: 4:1 MUX, 4-bit full adder,

- Ripple Counter

Behavioral Modeling
- Structured Procedures
- Procedural Assignment
- Timing Control
- Conditional statements
- Multiway branching
- Loops
- Sequential and parallel blocks
- Generate Blocks
- Design: 4:1 MUX, 4-bit counter,
- Traffic signal controller

Logic Synthesis and Verification
- What is logic synthesis?
- Impact of logic synthesis
- Verilog HDL synthesis
- Synthesis Design Flow
- Verification of Gate-level netlist
- Modeling tips for logic synthesis
- Design Partitioning
- Sequential Circuit Synthesis

Switch Level Modeling
- Switch modeling Elements
- MOS switches
- CMOS switches
- Design: CMOS NOR gate, 2:1 MUX, Simple CMOS Latch

Analog IC Design
- Fabrication Process of MOSFETs
- Introduction
- Basic steps
- CMOS Technology
- Layout Design Rules
- Layout design using Microwind
- Design: Logic Gates
- MOS inverter static characteristics
- Resistive Load Inverter
- CMOS inverter
- Design: CMOS Inverter design using
- Dsch and Microwind
- Importance of Time Delay and Low power

Models/Logics to be designed:
- 1-bit Half Adder
- 1-bit Full Adder
- 4-bit Ripple carry Full adder
- 4:1 MUX using logic equation
- 4:1 MUX using Conditional Operators
- 4:1 MUX using Dataflow Operators
- 4-bit Full adder using Dataflow Operators
- Ripple Counter
- Unidirectional Shift Register
- Bidirectional Shift Register
- T Flip-flop
- Edge triggered D FF
- 8:1 MUX with Case statement
- ALU Design
- Generated Ripple Adder
- Traffic Signal Controller
- Three Way Switch logic
- Task definition using ANSI C style Argument Declaration
- D-FF with Procedural Continuous Assignment
- Instantiation of a CMOS switch
- Switch level logic gates
- Serial Adder Design using FSM(Finite State Machine)
- MOD-8 counter using FSM
- Arbiter ckt using FSM
- Different types of sequence detector using FSM
- Synthesizable FIFO model (Project-1)
- Behavioral DRAM model (Project-2)
- Projects
- Synthesizable FIFO Model(Day-29)
- Behavioral DRAM Model(Day-30&31)
- Tools Used:
- Xilinx ISE Design Suite(For Digital IC Design)
- Microwind(For Analog IC Layout Design)
- Dsch(For Circuit Design)